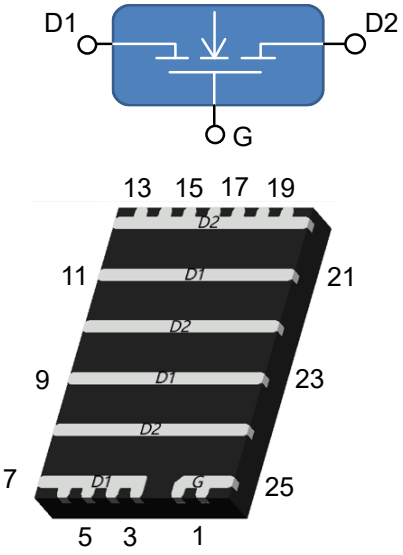
INV100FQ030A

1. General description

Bi-directional GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in FCQFN with 4.0 mm x 6.0 mm package size.



Bottom View

2. Features

- Bi-directional blocking capability
- GaN-on-Silicon E-mode HEMT technology
- Ultra-low on resistance

3. Applications

- BMS battery protection
- High side load switch in bi-directional converter
- Switch circuits in multiple power supplier system

4. Key performance parameters

Table 1 Key performance parameters at T_J = 25 °C

Parameter	Value	Unit
$V_{DD,\ max}$	100	V
$R_{DD(on),max}$ @ V_G = 5 V	3.2	mΩ
$Q_{G,typ}$ @ V_{DD} = 50V	90	nC
$I_{D,\ DC}$	100	A

5. Pin information

Table 2 Pin information

Pin	Pin description	Pin function
1,2,25	Gate	Driver Gate
3-7,9,11,21,23	Drain1	Power Drain1
8,10,12-20,22,24	Drain2	Power Drain2

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INV100FQ030A	FCQFN 4X6	J25

Table of contents

6. Maximum ratings

at T_J = 25 °C unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

SYMBOL	PARAMETER	MAX	UNIT
V_{DD}	Drain1-to-Drain2 Voltage or Drain2-to-Drain1 Voltage	100	V
$V_{DD(tr)}$	Drain1-to-Drain2 Voltage or Drain2-to-Drain1 Voltage [1] (V_{GD}=0V, 1h total time, T_A=T_{JMAX})	144	V
V_{DG}	Drain1-to-Gate Voltage or Drain2-to-Gate Voltage	100	V
V_{GD}	Gate-to-Drain1 Voltage or Gate-to-Drain2 Voltage	6	V
I_D	Continuous Drain Current (T_A = 25 °C)	100	A
I_{DM}	Pulsed Drain Current (25°C, T_{Pulse} = 100 µs)	320	A
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	°C

Note:

1. Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation;

7. Thermal characteristics

Table 5 Thermal characteristics

SYMBOL	PARAMETER	TYP	UNIT	Note/Test Condition
$R_{\theta JC}$	Thermal Resistance, Junction to Case	13.96	˚C/W	
$R_{\theta JB}$	Thermal Resistance, Junction to Board	1.92	˚C/W	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient [2]	57.56	˚C/W	
T_{sold}	Maximum reflow soldering temperature	260	°C	MSL3

Note:

2. $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

8. Electric characteristics

at T_J = 25 °C, unless specified otherwise

Table 6 Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
BV_{D1D2}	Drain1-to-Drain2 Breakdown Voltage	100	-	-	V	V_{D2} = V_G = 0 V, I_{D1D2} = 500 µA
BV_{D2D1}	Drain2-to-Drain1 Breakdown Voltage	100	-	-	V	V_{D1} = V_G = 0 V, I_{D2D1} = 500 µA
I_{D1D2}	Drain1-to-Drain2 Leakage	-	1	4	µA	V_{D2} = V_G = 0 V, V_{D1} = 80 V
I_{D2D1}	Drain2-to-Drain1 Leakage	-	1	4	µA	V_{D1} = V_G = 0 V, V_{D2} = 80 V
I_{GD}	Gate-to-Drain Forward Leakage	-	1	4	µA	V_{D1} = V_{D2} = 0 V, V_G = 5 V
	Gate-to-Drain Forward Leakage		2	8	µA	V_{D1} = V_{D2} = 0 V, V_G = 5.5 V
	Gate-to-Drain Forward Leakage	-	4.5	18	µA	V_{D1} = V_{D2} = 0 V, V_G = 6 V
$V_{GD1(TH)}$	Gate Threshold Voltage	0.8	1.1	2.5	V	V_{D1} = 0 V, V_{D2} = V_G, I_{D2D1} = 13 mA
$V_{GD2(TH)}$	Gate Threshold Voltage	0.8	1.1	2.5	V	V_{D2} = 0 V, V_{D1} = V_G, I_{D1D2} = 13 mA
$R_{D1D2(on)}$	Drain1-to-Drain2 On-state Resistance [3]	-	2.5	3.2	mΩ	V_{D2} = 0 V, V_{GD} = 5 V, I_{D1D2} = 25 A
$R_{D2D1(on)}$	Drain2-to-Drain1 On-state Resistance [3]	-	2.5	3.2	mΩ	V_{D1} = 0 V, V_{GD} = 5 V, I_{D2D1} = 25 A

Note:

3. $R_{D1D2(on)}$ and $R_{D2D1(on)}$ are measured without prior drain bias or switching stress.

Table 7 Dynamic characteristics [4]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{ISS}	Input Capacitance	-	3300	-	pF	V_G = 0 V, V_D = 50 V
C_{OSS}	Output Capacitance	-	830	-		
C_{RSS}	Reverse Transfer Capacitance	-	400	-		
R_G	Gate Resistance	-	5	-	Ω	f = 5 MHz，Open drain
Q_G	Total Gate Charge	-	90	-	nC	V_D = 50 V, V_G = 5 V, I_D = 25 A
Q_{GD1}	Gate-to-Drain1 Charge (V_{D2D1}=50V)	-	7	-		V_{D1} = 0, V_{D2} = 50 V, I_{D2D1} = 25 A
Q_{GD1}	Gate-to-Drain1 Charge (V_{D1D2}=50V)	-	65	-		V_{D2} = 0, V_{D1} = 50 V, I_{D1D2} = 25 A
Q_{GD2}	Gate-to-Drain2 Charge (V_{D1D2}=50V)	-	7	-		V_{D2} = 0, V_{D1} = 50 V, I_{D1D2} = 25 A
Q_{GD2}	Gate-to-Drain2 Charge (V_{D2D1}=50V)	-	65	-		V_{D1} = 0, V_{D2} = 50 V, I_{D2D1} = 25 A
Q_{OSS}	Output Charge	-	85	-		V_G = 0 V, V_D = 50 V

Note:

4. Guaranteed by design.

9. Electric characteristics diagrams

at T_J = 25 °C unless otherwise specified.

Note: In Charts, VD1D2 can be VD2D1 with same characteristic chart due to Bi-directional feature.

Fig. 1 Typical Output Characteristics (T_J=25°C)

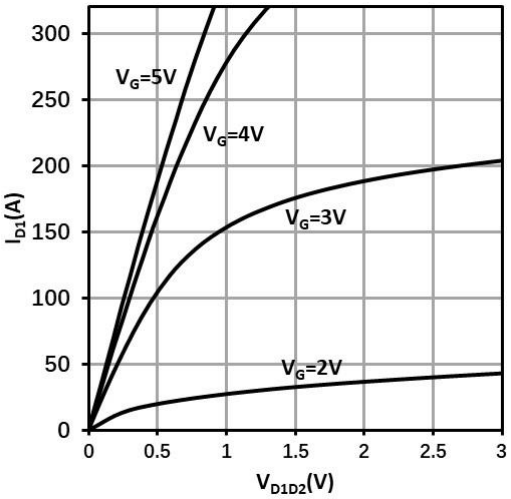


Fig. 2 Typical Output Characteristics (T_J=125°C)

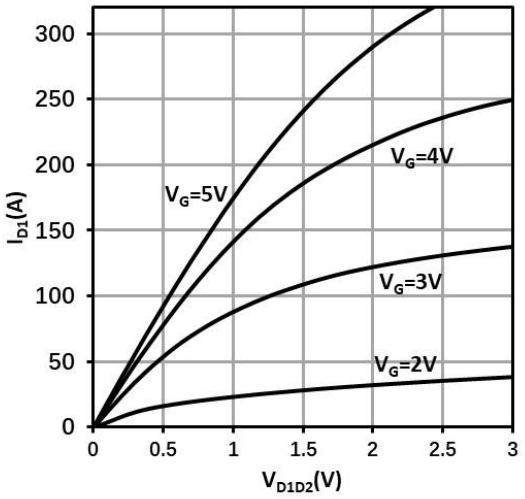


Fig.3 Typical Drain On-state Resistance (T_J=25°C)

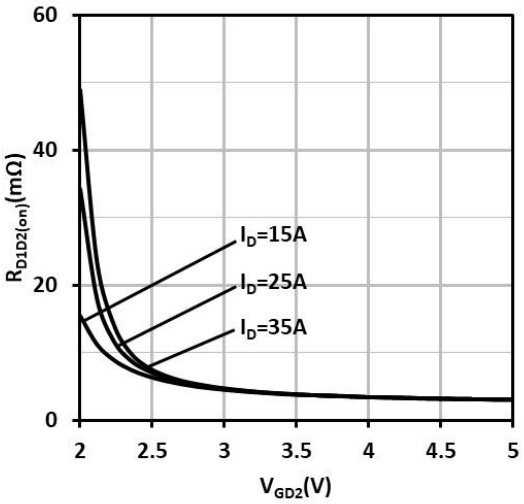


Fig. 4 Typical Drain On-state Resistance (T_J=125°C)

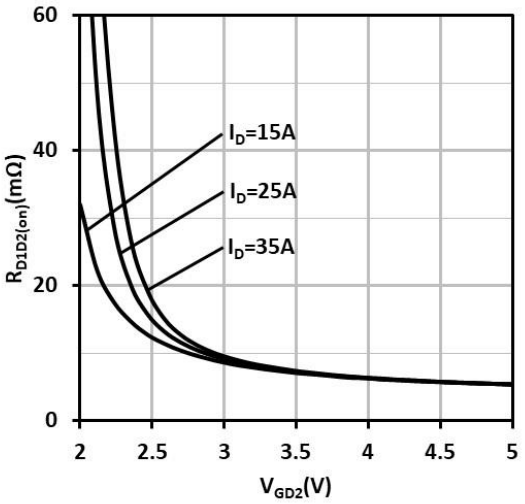


Fig. 5 Normalized On-State Resistance vs. Temp.

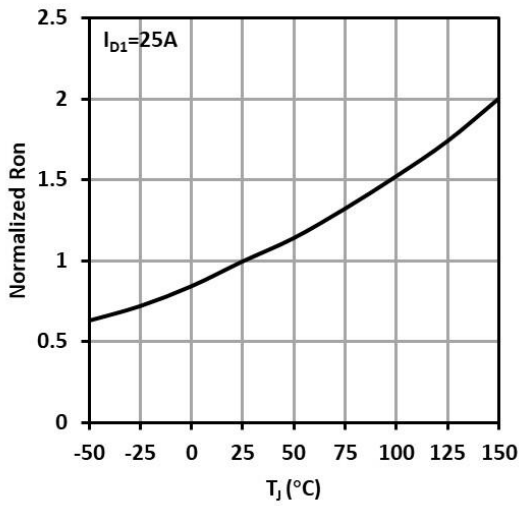


Fig. 6 Typical Transfer Characteristics

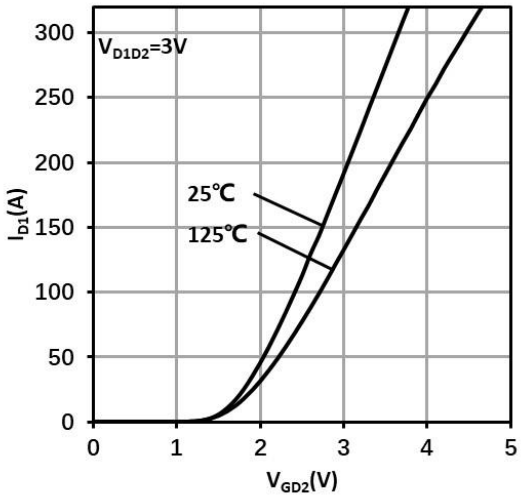


Fig. 7 Typ. Reverse Drain1-Drain2 Characteristics (V_{GD2}≤0,T_J =25°C)

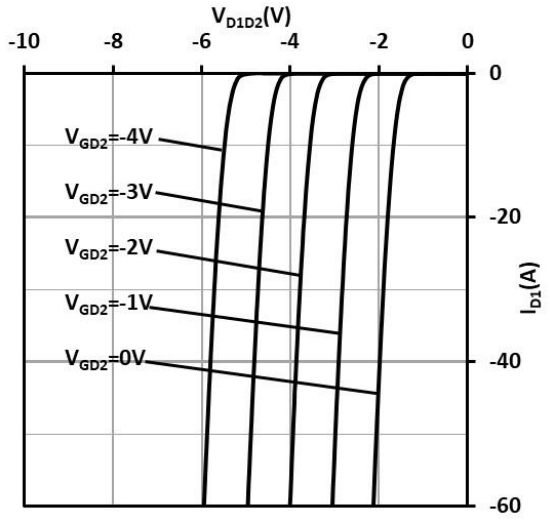


Fig. 8 Typ. Reverse Drain1-Drain2 Characteristics (V_{GD2}≥0,T_J =25°C)

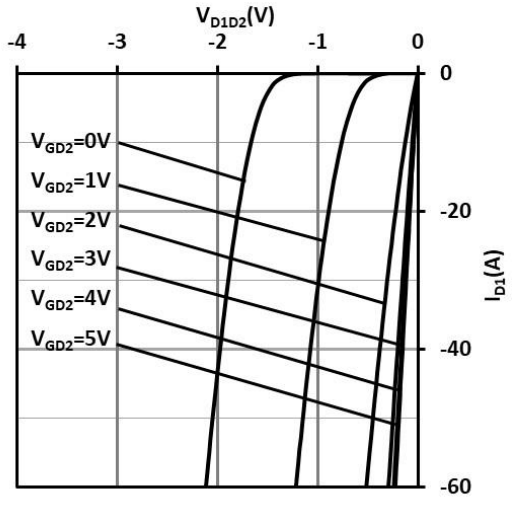


Fig. 9 Typ. Reverse Drain1-Drain2 Characteristics (V_{GD2}≤0, T_J = 125 °C)

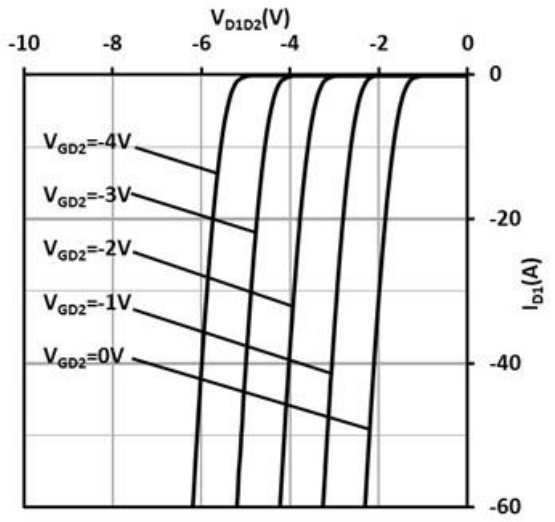


Fig. 10 Typ. Reverse Drain1-Drain2 Characteristics (V_{GD2}≥0,T_J = 125 °C)

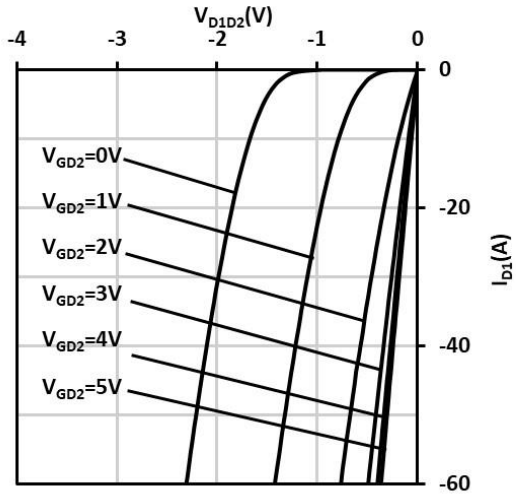


Fig. 11 Typ. Capacitances Characteristics

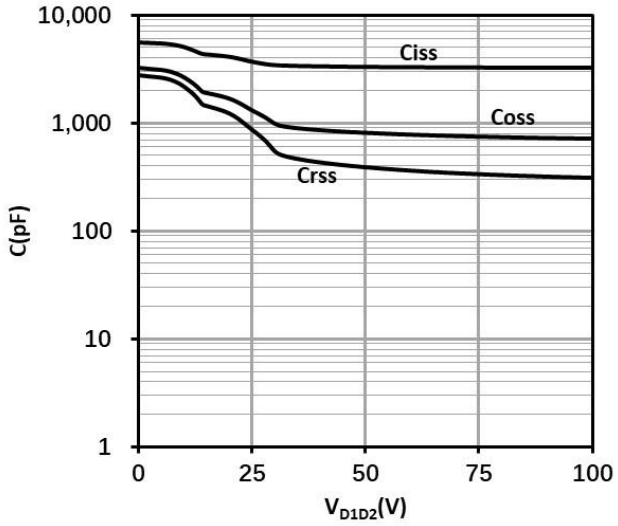


Fig. 12 Typ. Gate Charge

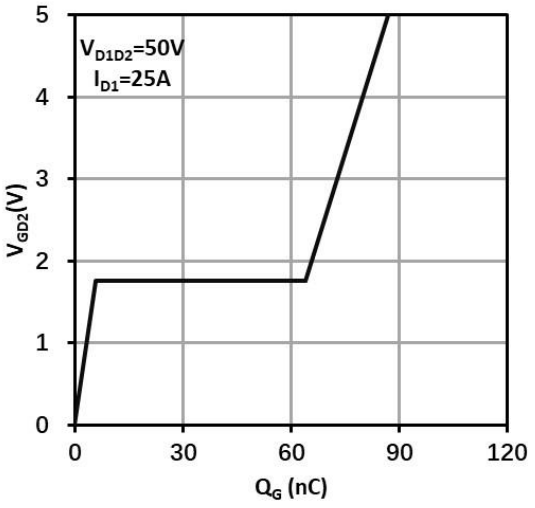


Fig. 13 Normalized Threshold Voltage vs. Temp.

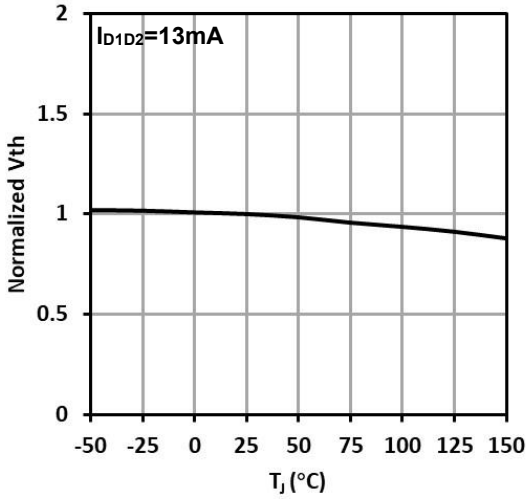


Fig. 14 Output Charge

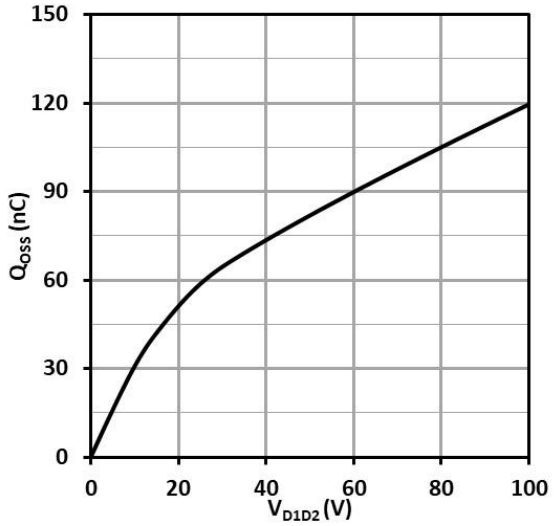


Fig. 15 Output Capacitance Stored Energy

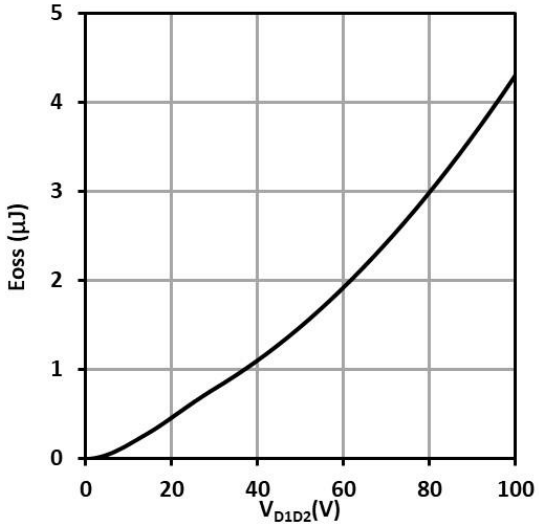


Fig. 16 Power Dissipation

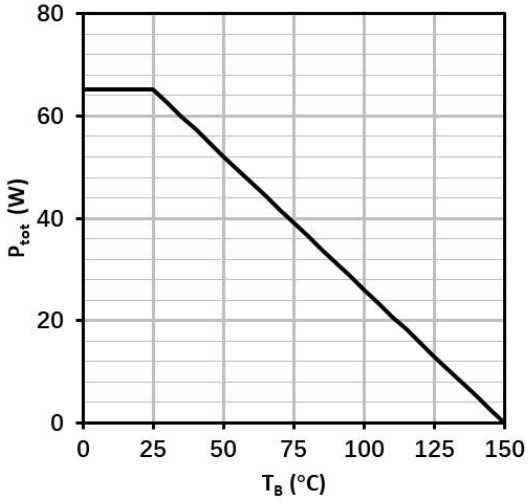


Fig. 17 Safe Operating Area

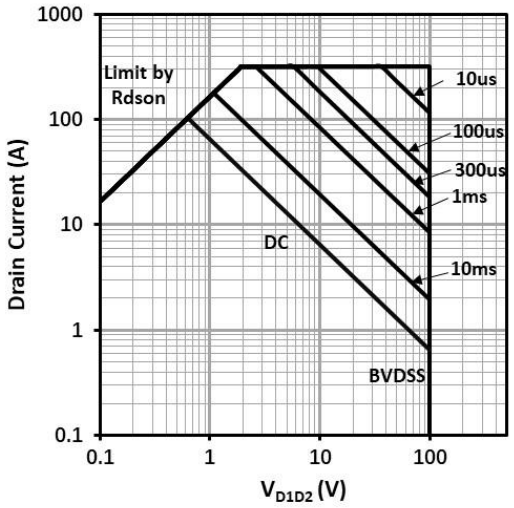
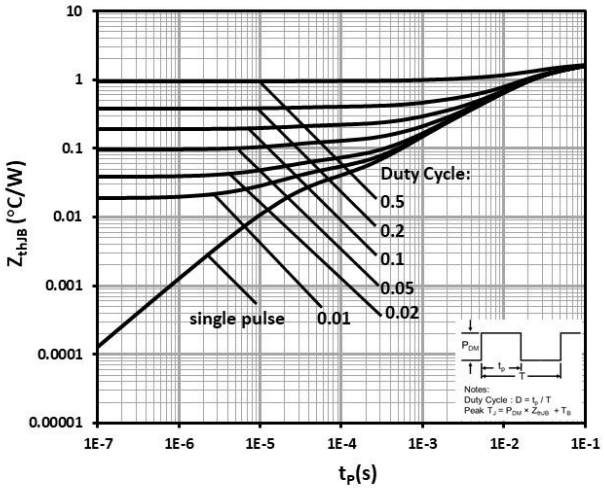
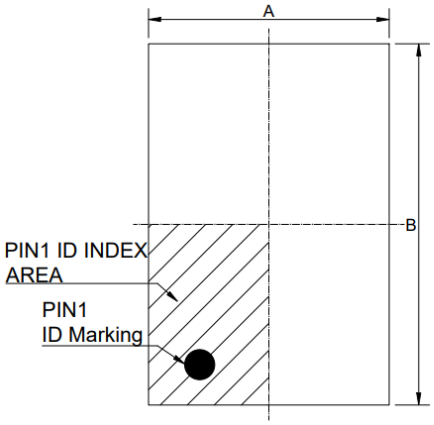


Fig. 18 Max. Transient Thermal Impedance

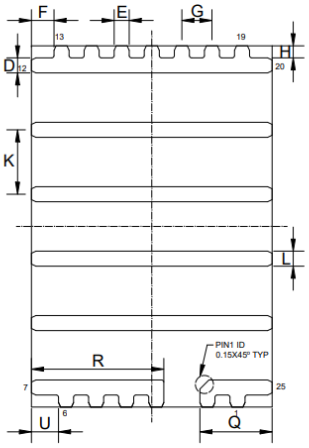


10. Package outlines

Package Reference



TOP VIEW



BOTTOM VIEW

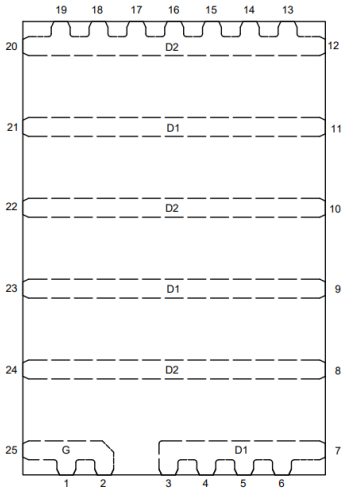
SYMBOL	MILLIMETER			NOTE
	MIN	NOM	MAX	
A	3.9	4.0	4.1	
B	5.9	6.0	6.1	
D	0.20	0.25	0.30	3X
E	0.20	0.25	0.30	13X
F		0.375 REF		2X
G		0.5 BASIC		10X
H		0.2 REF		3X
K		1.07 BASIC		6X
L	0.20	0.25	0.30	4X
Q	1.1	1.2	1.3	
R	2.1	2.2	2.3	
U		0.45 REF		2X
Z		0.203 REF		
AA	0.75	0.85	0.95	
AB	0.00	0.02	0.05	

SIDE VIEW

NOTE:

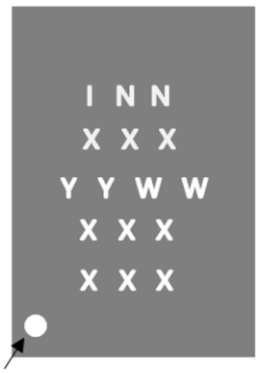
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

PIN configuration



TOP VIEW

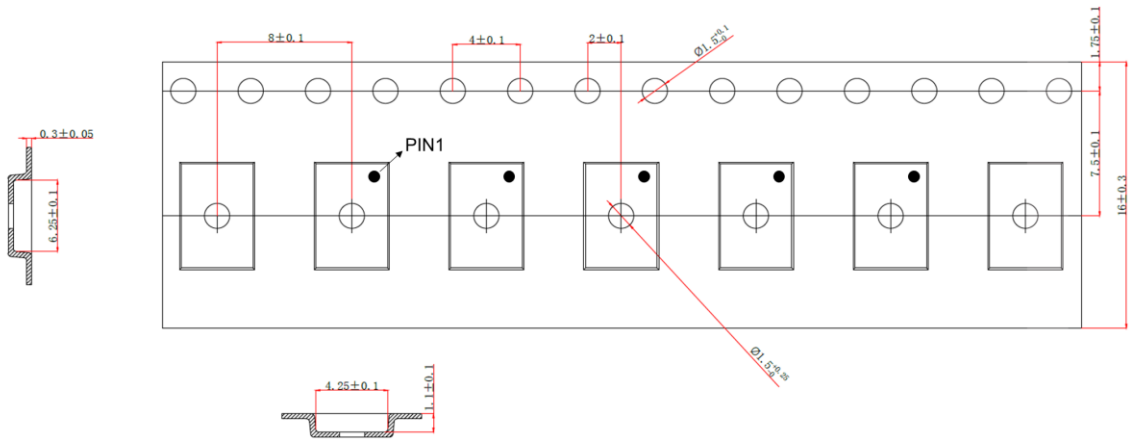
Marking Reference



Die Orientation Dot
&Gate Position

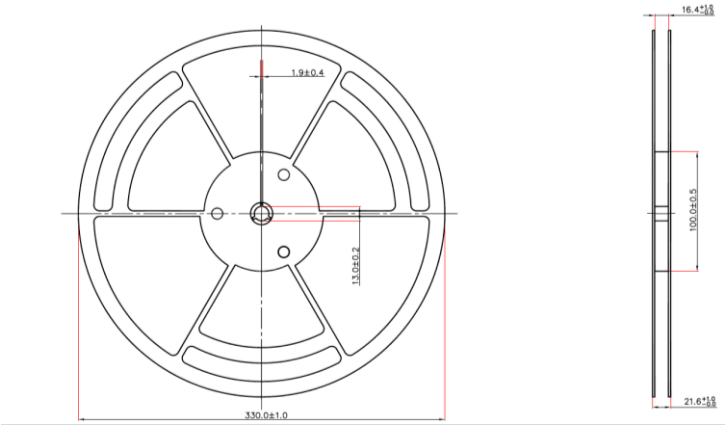
Row	Description	Example
Row 1	Company name	INN
Row 2	Product code	XXX
Row 3	Date code	YYWW
Row 4	Lot No	XXX
Row 5	Lot No	XXX

11. Reel information



NOTES:

1. CARRIER TAPE COLOR: BLACK.
2. COVER TAPE WIDTH: 13.3±0.10.
3. COVER TAPE COLOR: TRANSPARENT.
4. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.20 MAX.
5. CAMBER NOT TO EXCEED 1MM IN 100MM.
6. MOLD# QFN/DFN/MIS6X4X0.75/0.85.
7. ALL DIMS IN MM.
8. BAN TO USE THE ENVIRONMENT-RELATED SUBSANCES OF JCET PRESCRIBING.

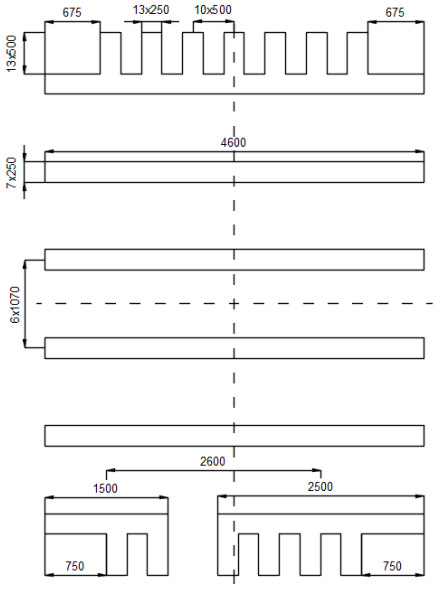


NOTES:

1. 2500 UNITS PER TRAY.
2. COLOR: WHITE.
3. ALL DIM IN mm.
4. GENERAL TOLERANCE±0.25.
5. BAN TO USE THE ENVIRONMENT-RELATED SUBSANCES OF JCET PRESCRIBING.
6. THE DERECTION OF VIEW:

12. Land pattern

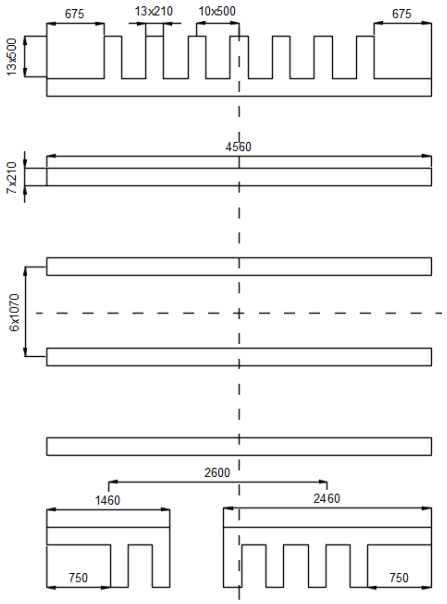
Recommended Land Pattern



TOP VIEW

Unit:μm

Recommended Stencil drawing



TOP VIEW

Unit:μm

13. Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2023-11-24	Version 1.0 release
1.1	2024-12-16	1. Update $V_{DD(tr)}$ from 120V to 144V in table 4, and update the test condition; 2. Add note in table 4,6,7; 3. Add Pin1 location in reel information.

Important Notice

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